Zhongchun Zheng · 郑中淳

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Education

Sun Yat-sen University B.E. · MA.Eng in Computer Science 2019/09 - 2026/06 (expected)

- Supervised by X. Zhang, interested in **compiler** and **Machine Learning**.

Research

VecTrans: LLM Transformation Framework for Better Auto-vectorization on High-performance CPU

Z. Zheng, L. Cheng, L. Li, R. Rocha, T. Liu, W. Wei, X. Zhang, Y. Gao. LCTES'25 submitted

- VecTrans leverages LLMs to enhance compiler-based code vectorization.
- VecTrans first employs compiler analysis to identify potentially vectorizable code regions. It then utilizes an LLM to refactor these regions into patterns that are more amenable to the compiler's auto-vectorization.

mLOOP: Optimize Loop Unrolling in Compilation with a ML-based Approach

Z. Zheng, Y. Wu, X. Zhang. GitHub. NAS'24

- mLOOP employs the XGBoost model to predict loop unroll factors.
- mLOOP is implemented as an LLVM optimization pass, enabling seamless deployment within existing compiler pipelines.

GoPTX: Fine-grained GPU Kernel Fusion by PTX-level Instruction Weaving

K. Wu, Z. Lin, X. Meng, Z. Zheng, W. Pan, X. Zhang, Y. Lu. GitHub. DAC'25

REFIT: Improve Code Efficiency via Binary Level Loop Optimization

T. Zhang, G. Chen, W. Pan, Z. Zheng, G. Sun and X. Zhang. ICCCS'25

Research Interest

Compiler Optimizations & ML-Augmented Code Generation

- Focus on synergistic techniques between compiler optimizations (e.g., **loop unrolling, vectorization**) and machine learning, enhancing performance in HPC and edge computing.
- Future work: **Repository-level code optimization** (cross-procedural/inter-file analysis) and **scalable parallel code generation** for heterogeneous architectures (CPU/GPU/TPU).

Experience

Huawei 2012 Lab, Compiler Engineer (Intern) 2024/08 - now

Sun Yat-sen University, School of Computer Science 2024/02 - 2024/07

Teach Assistant for DCS292 - Compiler Construction. YatCC

Developed and guided course materials for compiler design, with key contributions to:

- Experiment 3 (IR Generation) –Translating AST to LLVM IR.
- Experiment 4 (Optimization) –Implementing and analyzing IR-level optimizations.
- Pioneered the integration of LLMs to assist in code generation and optimization.

Honor

First-Prize Scholarship, Sun Yat-sen University	2024/10
First Prize, Best Teaching Case, China Computer Education Conference(CCEC'24)	2024/07
Second-Prinze, Greater Bay Area Cup AI for Science Technology Competition	2023/11
First-Prize, Huawei Bisheng Cup Compiler System Design Competition (CSC)	2023/08
CCF Elite Collegiate Award (102 in China), China Computer Federation (CCF)	2022/09
Top 5%, CCF Certified Software Professional	2022/06
Gold Award,iGEM Competition	2022/04
Second-Prize Scholarship, Sun Yat-sen University	2021/10